SSI Specification Micro Module Server

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Revision 1.1.0

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Revision History

The following table lists the revision schedule based on revision number and development stage of the product.

Revision	Project Document State	Date
0.10	First draft for internal review.	12/07/09
0.30	Draft proposal for external review.	12/23/09
0.80	Final content ready for partner review	4/10
0.85	Final content ready for member review	8/10
1.0	First public release	10/10
1.1	Updated public release	4/12

Note: Not all revisions may be published.

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1 Introduction

1.1 Purpose

This *SSI Micro Module Server Specification* is intended to define a server board (aka Micro Module or µModule) form factor and connector. A micro server is an emerging server category that is generally described as a scale-out single socket, entry level, low cost, low power, improved density / efficiency and "good enough" performance server.

This specification encompasses board size, connector design, and connector pin out for two form factors relevant to the Micro Server segment. It also provides examples and guidelines for thermal design.

1.2 Scope

This revision of the Micro Module Specification is optimized for one to four compute nodes per module, where a compute node consists of a uniprocessor (single socket) server processor, memory, and I/O controllers.

1.3 Form Factors

Two form factors are proposed for the Micro Module Server

Top Access µModule – This form factor uses a card-edge connector on the long edge of the board for plugging µModules from the top of a chassis into a system baseboard.

Front Access µModule – This form factor uses a card-edge connector on the short edge of the board to allow for plugging µModules from the front of a chassis into a system backplane or midplane.

1.4 Audience

The primary audience for this specification is:

Platform / System Architects

Hardware Design Engineers

Product Line Managers

System Technologists and Planners

Test and Validation Engineers

Marketing Engineers and Planners

1.5 Specification Compliance

Products making the claim of compliance with this specification **shall** provide, at a minimum, all features defined as mandatory by the use of the keyword "**shall**". Such products **may** also provide recommended features associated with the keyword "**should**" and permitted features associated with the keyword "**may**".

1.6 Reference Documents

Note: Later revisions of the following specifications are allowed assuming backwards compatibility is maintained.

IEEE Std 802.3ap-2007 "Backplane Ethernet" standard.

IPMI – Intelligent Platform Management Interface Specification, v2.0 rev 1.0E3, February 16, 2006, Copyright © 2004, 2005, 2006 Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Inc., All rights reserved.

PCIe - PCI Express® Base Specification Revision 2.0, December 20, 2006, PCI-SIG®, all rights reserved.

PCIe - PCI Express® Card ElectroMechanical Specification Revision 2.0, April 11, 2007, PCI-SIG®, all rights reserved.

Serial ATA Specification, Revision 1.0a. (and later revisions)

Universal Serial Bus Specification (USB), Revision 2.0.

1.7 Terms and Abbreviations

The following terms and acronyms are used in specific ways throughout this specification:

Table 1-1: Terms and Abbreviations

Term	Definition
BMC	Baseboard Management Controller. A management controller local to the Micro Module Server. A BMC is typically IPMI compliant. A BMC is typically implemented for a single node, but can be implemented to support multiple nodes.
CFM	Cubic Feet per Minute. A measure of volumetric airflow. One CFM is equivalent to 472 cubic centimeters per second.
Chassis	The mechanical enclosure that consists of the baseboard or midplane, Micro Module Servers, cooling devices, power supplies, hard disk drives, etc. The chassis provides the interface to boards and consists of the guide rails, alignment, handle interfaces, face plate mounting hardware, etc.
Component side	When used in reference to a PBA, the side on which the tallest electronic components such as the CPU and DIMMs would be mounted. Also called the Primary Side.
Guide Rail	May provide for the Micro Module Server board guidance feature in a slot.
HDD	Hard Disk Drive (magnetic)

Term	Definition
Intelligent Platform Management Bus (IPMB)	IPMB is an I^2C-based bus that provides a standardized interconnection between managed modules within a chassis. ftp://download.intel.com/design/servers/ipmi/ipmb1010ltd.pdf
Intelligent Platform Management Interface (IPMI)	IPMI v2.0 R1.0 specification defines a standardized, abstracted interface to the platform management subsystem of a computer system. ftp://download.intel.com/design/servers/ipmi/IPMIv2_0rev1_0.pdf
Interconnect Channel	An interconnect channel is comprised of two pairs of differential signals. One pair of differential signals for transmit and another pair of differential signals for receive.
Link	Network link representing either a single channel or aggregation of channels (example: KX4 using 4 channels would be a single Link). The term “Link” does not represent virtualized aggregation such as “teaming”.
LFM	Linear Feet per Minute. A measure of air velocity. One LFM is equivalent to 0.508 centimeters per second.
may	Indicates flexibility of choice with no implied preference.
Midplane	Equivalent to a system backplane. This is a PBA that provides the common electrical interface for a chassis in which server and interface boards plug into the front and rear of the chassis.
Module	A physically separate chassis component that may be independently replaceable (e.g., a µModule Server or cooling module) or attached to some other component (e.g., a baseboard).
Node	A self-contained compute server. Multiple nodes can be implemented on a µModule.
PBA	Printed board assembly. A printed board assembly is a printed circuit board that has all electronic components attached to it.
PCB	Printed circuit board without components attached.
PCIe	PCI Express®
SATA	Serial ATA (Advanced Technology Attachment). A storage interface for connecting host bus adapters to mass storage devices such as hard disk drives and optical drives
Secondary side	When used in reference to a PBA, the side normally reserved for making solder connections with through-hole components on the Component Side but on which low height electronic components may also be mounted.
SERDES	Serializer/Deserializer. In this case SERDES refers to the full duplex differential pair signaling specified by the IEEE 802.3ap backplane Ethernet specifications.
Shall	Indicates a mandatory requirement. Designers must implement such mandatory requirements to ensure interchangeability and to claim conformance with this specification. The use of **shall not** indicates an action or implementation that is prohibited.
Should	Indicates flexibility of choice with a strongly preferred implementation. The use of **should not** indicates flexibility of choice with a strong preference that the choice or implementation be avoided.
Slot	A slot defines the position of one Micro Module Server in a chassis.
SSD	A solid-state drive (SSD) is a data storage device that uses solid-state memory to store persistent data. Used in place of a hard disk drive.
U	Unit of vertical height defined in IEC 60297-1 rack, shelf, and chassis height increments. 1U=1.75 inches.

Term	Definition
USB	Universal Serial Bus
µModule	Micro Module Server defined by this specification
VR	Voltage Regulator. The µModule is supplied 12VDC on the connector and requires local voltage regulation to derive all logic voltages.

2 µModule Architecture

2.1 Micro Module Server Goals

The overall goal is to define a standard that will make it easier for the industry to build products with a defined board outline and connector interface, enabling lower costs and a reduced time-to-market. As such, the standard will provide flexible specification that maximizes design leverage while providing ample room for OEM/ODM differentiation.

Two form factors are defined, one targeted on top access, the other on front access.

2.1.1 High-level Strategic Goals

The following are the high-level strategic goals of the µModule specification:

- Common connector interface to maximize design re-use
- Flexibility to enable industry innovation and OEM value add
- Form factor that maximizes density at the lowest cost
- Enable multi-computer servers, lowering total cost of ownership
- Limit standard to the most basic compute elements and I/O
- Target uniprocessor (single socket)
    - low power, “good enough” server CPU performance for scale out applications
    - higher power single node for specific performance sensitive applications that may also require more memory
- Leave system feature and mechanical implementation to OEMs, i.e. system interconnect , storage topology, chassis management , hot-plug, chassis size, module pitch etc.
-

2.1.2 High-level Technical Goals

The following are the high-level technical goals of the µModule specification:

- Utilize proven high-volume connectors for low cost and TTM
- Enable rack mount chassis with either front or rear I/O access
- Optimized density/scalability for a range of rack power
- Industry standard management interface options
- Shared system resources for cost/power reduction
    - Power, cooling, management module
- Off-module I/O resources to enable small form factor and flexible system design
    - HDD/SDD, network switching & PHY, virtual KVM & media, USB connectors
- Two-tiered compatible connector approach
    - “Base” connector for basic computing elements

- "Extended" connector for higher I/O capabilities and OEM/ODM differentiation

2.2 Power Envelope

Although the maximum power for each form factor is defined, the power consumption of the system containing a µModule is not constrained by this specification. Thermal design of the system is the responsibility of the OEM.

2.3 µModule Connector Signal Groups

The µModule's connector signals are categorized into functional groups. Three groups are required while the others are optional. All signal locations **shall** be used only for the functions specified; they **shall not** be repurposed. See sections **Error! Reference source not found.** and 4.2.1 for a graphical overview of the connector signal groups for the top access and front access µModules.

2.3.1 12V Power

Only 12V is delivered to the µModule through the baseboard or backplane connector. All main power rails **shall** be derived from the 12V rail.

2.3.2 Power Control

PRSNT0# and PRSNT1# are for µModule card presence detect. One present detect pin (with short edge finger contact) at each end of the base connector guarantees that at least one of the present detect pins is last-mate/first-break. This function can be used to enable hot-plug operations on the µModule by enabling/disabling power rails during plug/unplug operation. The PRSNT# signals are connected on the µModule. The system baseboard provides a pull-up resistor on one of the PRSNT# pins and grounds the other pin as shown in section 3.2 of *PCI Express® Base Specification Revision 2.0*

Note that the PRSNT# pins are not located at the same positions as on standard PCI Express connectors, and that CAD symbols must be modified to place the contacts with short pads at the correct pin positions as defined by this specification.

PWR_BTN# is an (active low) input indicating that a power button has been depressed to request a change to the µModule power state. This signal can also be asserted by a system management controller to control the power state of the µModule.

2.3.3 SSI Reserved Pins

SSI reserved pins on the connector definition are intended for future use. Systems **shall not** use the reserved pins for proprietary use. These pins **shall** remain unconnected.

2.3.4 SATA

The Micro Module Server supports multiple SATA mass storage devices as defined by the Serial ATA Specification, Revision 1.0a and later revisions. The directions of the high-speed signals are defined as "µModule"-centric. As defined by the µModule interface connector, the transmit pairs on the connector **shall** connect to the transmit pins on the µModule's SATA controller. Similarly, the receive pins on the connector **shall** connect to the receive pins on the µModule's SATA controller. It is the responsibility of the system designer to properly connect the transmit pins from the µModule to the receive pins on the SATA device(s) in the system.

2.3.5 3.3V Out

A 3.3V output pin is defined to provide power for functions directly related to a module. For example, SATA signals may require a re-driver located off the module which may be powered by this 1A source. Another possible use is to illuminate a power LED located off the module. This pin also provides indication that the power rails on the µModule are turned on, which may be used to turn on external voltage regulators for devices associated with this µModule (e.g. a PCIe device).

2.3.6 Identify

Two signals are provided to help identify a specific module in a system. The ID Button signal is an input that when active, causes the µModule to illuminate an ID LED. The ID LED signal is an output that provides the state of the module's ID LED to the backplane.

2.3.7 Slot ID

SLOT_ID_(5:0) provide strapping to the µModule to allow for uniquely identifying the physical slot in the system. These strapping pins should be routed to the µModule BMC or other management resources to provide unique system level management addressing.

The choice on how to physically number the slots in a system is system design responsibility.

2.3.8 I2C Management

There are two types of I2C buses on the connector for management.

IPMB_CLK and IPMB_DAT is an I2C bus that may optionally be used as an IPMI compliant management bus connecting a chassis or system level management entity to a Baseboard Management Controller (BMC) on the µModule. While IPMB management is not required, a system that uses IPMB should use this i2c bus for the function.

SMBus_CLK and SMBus_DAT is an I2C bus that may optionally be used to communicate with slave devices located outside the module. Example devices might include temperature, fan or voltage sensors, a hot-swap controller, or PCIe add-in cards. This I2C bus may also be used to connect a chassis or

system level management entity to a BMC on the module if the management architecture is not using IPMB.

2.3.9 SERDES

The SSI Micro Module Server supports multiple backplane Ethernet SERDES interfaces. The basic parameters for the signals are defined in the IEEE Std. 802.3ap-2007 “Backplane Ethernet” standard.

The directions of the high-speed signals are defined as “µModule”-centric. As defined by the µModule interface connector, the transmit pairs on the connector **shall** connect to the transmit pins on the µModule’s Ethernet controller. Similarly, the receive pins on the connector **shall** connect to the receive pins on the µModule’s Ethernet controller. It is the responsibility of the system designer to properly connect the transmit pins from the µModule to the receive pins on the switch module or PHY interface in the system.

Two LED signals are outputs associated with the network ports: ACT_LED_A# and ACT_LED_B# are (active low) LED indicator signals for Link Activity. These signals indicate activity on each of the SERDES Ethernet links controlled by µModule. Note: these signals are only present on the top access µModule connector. Activity LEDs for the front access µModule may be present on the module faceplate.

2.3.10 Management LAN

The management LAN group is for optional, dedicated management LAN(s). This LAN is a 100BASE-TX, point-to-point, full duplex interconnect.

The directions of the high-speed signals are defined as “µModule”-centric. As defined by the µModule interface connector, the transmit pairs on the connector **shall** connect to the transmit pins on the µModule’s Ethernet controller. Similarly, the receive pins on the connector **shall** connect to the receive pins on the µModule’s Ethernet controller. It is the responsibility of the system designer to properly connect the transmit pins from the µModule to the receive pins on the switch module or PHY interface in the system.

For backplane applications, it is common practice to use capacitive AC coupling verses magnetics. To do so typically requires Auto-Negotiation and Auto MDI/MDIX to be disabled. Some PHYs may not support capacitive coupling. Refer to the PHYs manufacturer documentation for implementation details.

An LED signal is associated with the management LAN: MNGT_ACT_LED# is an (active low) LED indicator output signal for the Management LAN Link Activity. This signal indicates activity on the management Ethernet links controlled by µModule. Note: this signal is only present on the top access µModule connector. An activity LED for the front access µModule may be present on the module faceplate.

2.3.11 PCI Express®

The top access µModule supports PCI Express® on the module connectors. The PCI Express® signals conform to *PCI Express® Base Specification Revision 2.0*. The x8 lanes on the top access µModule base connector can be bifurcated into two x4 lane segments using the two available clock pairs (PE_CLK_0 and PE_CLK_1). This is allowed if the x4 lanes on the extended connector (optional reference pinout) are not used. The x4 lanes on the extended connector are available for a secondary device in addition to the x8 lanes on the base connector. Only two PCIe end segments are supported from both the base connector and the extended connector, since there are two available clock pairs.

- The directions of the high-speed signals are defined as "µModule"-centric. The receiver differential pair of the connector **shall** be connected to the PCI Express Receiver differential pair of the µModule controller, and to the PCI Express Transmitter differential pair on PCI Express device off the µModule. The transmitter differential pair of the connector **shall** be connected to the PCI Express Transmitter differential pair on the µModule PCI Express controller, and to the PCI Express Receiver differential pair on PCI Express device off the µModule.
- The "P" and "N" connections **may** be reversed to simplify PCB trace routing and minimize vias if needed. All PCI-Express Receivers incorporate automatic Lane Polarity Inversion as part of the Link Initialization and Training and will correct the polarity independently on each Lane. Refer to Section 4.2.4 of the *PCI Express Base Specification, Revision 2.0*.
- Support for PCI Express Lane Reversal is optional on the µModule.

Note: Conformance to the PCIe specification and other open standards does not imply that erratum does not exist with the control chipsets.

2.3.12 USB

The top access µModule supports up to two USB devices as defined by the Universal Serial Bus Specification (USB), Revision 2.0.

The directions of the high-speed signals are defined as "µModule"-centric. As defined by the µModule interface connector, the transmit pairs on the connector **shall** connect to the transmit pins on the µModule's USB controller. Similarly, the receive pins on the connector **shall** connect to the receive pins on the µModule's USB controller. It is the responsibility of the system designer to properly connect the transmit pins from the µModule to the receive pins on the USB device(s) in the system.

2.3.13 OEM / Future Use

This group is left undefined in the specification and may be used for OEM specific functions. This group may also be defined in future revisions of the specification. Feedback from µModule OEMs on features useful for the base connectors may be incorporated onto these pins in the future.

2.3.14 OEM Defined

The extended connector contains pins left up to the OEM to define. Optional reference pinouts for the top access and front access µModules are provided for OEMs and ODMs that would prefer to maximize design leverage across multiple board designs and system implementations.

2.4 µModule Connector Signal Definition

The signals present on the top access µModule and front access µModule are not identical. There may be multiple copies of some signals (such as IPMB_CLK and IPMB data) on the front access connector in order to support multiple nodes. Refer to the pinout tables for each form factor in its respective section.

Table 2-1: µModule Connector Signal Definitions

Signal Name	Signal Description	Signal Group
12V	12VDC Power Supply Pins	12V Power
3.3V_OUT	3.3V Output (1A source)	3.3V Out
ACT_LED_A#	NIC Activity LED (active low) for SERDES A	SERDES
ACT_LED_B#	NIC Activity LED (active low) for SERDES B	SERDES
GND	Ground Pins	Ground
ID_BTN#	ID button pressed Input (active low)	Identify
ID_LED#	Module ID illuminated output (active low)	Identify
IPMB_CLK	IPMB Bus Serial Clock	I2C Management
IPMB_DAT	IPMB Bus Serial Data	I2C Management
MNGT_ACT_LED#	Management NIC Activity LED (active low)	Management LAN
MNGT_RX_DN	RX- of Mngt LAN	Management LAN
MNGT_RX_DP	RX+ of Mngt LAN	Management LAN
MNGT_TX_DN	TX- of Mngt LAN	Management LAN
MNGT_TX_DP	TX+ of Mngt LAN	Management LAN
OEM Defined	Defined by OEM	OEM Defined
OEM/Future Use	Defined by OEM / May be used in future	OEM/Future Use
PCIE_PERST#	PCIe Fundamental Reset output	PCI Express
PCIE_WAKE#	PCIe Wake# input	PCI Express
PE_A_RX_0_DN	RX- of Base PCIe Lane 0	PCI Express
PE_A_RX_0_DP	RX+ of Base PCIe Lane 0	PCI Express
PE_A_RX_1_DN	RX- of Base PCIe Lane 1	PCI Express
PE_A_RX_1_DP	RX+ of Base PCIe Lane 1	PCI Express
PE_A_RX_2_DN	RX- of Base PCIe Lane 2	PCI Express
PE_A_RX_2_DP	RX+ of Base PCIe Lane 2	PCI Express
PE_A_RX_3_DN	RX- of Base PCIe Lane 3	PCI Express
PE_A_RX_3_DP	RX+ of Base PCIe Lane 3	PCI Express
PE_A_RX_4_DN	RX- of Base PCIe Lane 4	PCI Express
PE_A_RX_4_DP	RX+ of Base PCIe Lane 4	PCI Express
PE_A_RX_5_DN	RX- of Base PCIe Lane 5	PCI Express

PE_A_RX_5_DP	RX+ of Base PCIe Lane 5	PCI Express
PE_A_RX_6_DN	RX- of Base PCIe Lane 6	PCI Express
PE_A_RX_6_DP	RX+ of Base PCIe Lane 6	PCI Express
PE_A_RX_7_DN	RX- of Base PCIe Lane 7	PCI Express
PE_A_RX_7_DP	RX+ of Base PCIe Lane 7	PCI Express
PE_A_TX_0_DN	TX- of Base PCIe Lane 0	PCI Express
PE_A_TX_0_DP	TX+ of Base PCIe Lane 0	PCI Express
PE_A_TX_1_DN	TX- of Base PCIe Lane 1	PCI Express
PE_A_TX_1_DP	TX+ of Base PCIe Lane 1	PCI Express
PE_A_TX_2_DN	TX- of Base PCIe Lane 2	PCI Express
PE_A_TX_2_DP	TX+ of Base PCIe Lane 2	PCI Express
PE_A_TX_3_DN	TX- of Base PCIe Lane 3	PCI Express
PE_A_TX_3_DP	TX+ of Base PCIe Lane 3	PCI Express
PE_A_TX_4_DN	TX- of Base PCIe Lane 4	PCI Express
PE_A_TX_4_DP	TX+ of Base PCIe Lane 4	PCI Express
PE_A_TX_5_DN	TX- of Base PCIe Lane 5	PCI Express
PE_A_TX_5_DP	TX+ of Base PCIe Lane 5	PCI Express
PE_A_TX_6_DN	TX- of Base PCIe Lane 6	PCI Express
PE_A_TX_6_DP	TX+ of Base PCIe Lane 6	PCI Express
PE_A_TX_7_DN	TX- of Base PCIe Lane 7	PCI Express
PE_A_TX_7_DP	TX+ of Base PCIe Lane 7	PCI Express
PE_B_RX_0_DN	RX- of Extended PCIe Lane 0	PCI Express
PE_B_RX_0_DP	RX+ of Extended PCIe Lane 0	PCI Express
PE_B_RX_1_DN	RX- of Extended PCIe Lane 1	PCI Express
PE_B_RX_1_DP	RX+ of Extended PCIe Lane 1	PCI Express
PE_B_RX_2_DN	RX- of Extended PCIe Lane 2	PCI Express
PE_B_RX_2_DP	RX+ of Extended PCIe Lane 2	PCI Express
PE_B_RX_3_DN	RX- of Extended PCIe Lane 3	PCI Express
PE_B_RX_3_DP	RX+ of Extended PCIe Lane 3	PCI Express
PE_B_TX_0_DN	TX- of Extended PCIe Lane 0	PCI Express
PE_B_TX_0_DP	TX+ of Extended PCIe Lane 0	PCI Express
PE_B_TX_1_DN	TX- of Extended PCIe Lane 1	PCI Express
PE_B_TX_1_DP	TX+ of Extended PCIe Lane 1	PCI Express
PE_B_TX_2_DN	TX- of Extended PCIe Lane 2	PCI Express
PE_B_TX_2_DP	TX+ of Extended PCIe Lane 2	PCI Express
PE_B_TX_3_DN	TX- of Extended PCIe Lane 3	PCI Express
PE_B_TX_3_DP	TX+ of Extended PCIe Lane 3	PCI Express
PE_CLK_1_DN	CLK- of PCIe Clock 1	PCI Express
PE_CLK_1_DP	CLK+ of PCIe Clock 1	PCI Express
PE_CLK_2_DN	CLK- of PCIe Clock 2	PCI Express
PE_CLK_2_DP	CLK+ of PCIe Clock 2	PCI Express
PRSNT0#	uModule Present 0 (active low, short pin)	Power Control
PRSNT1#	uModule Present 1 (active low, short pin)	Power Control
PWR_BTN#	Power Button Input (active low)	Power Control
RSVD	Reserved for future use. Do not use.	SSI Reserved
SATA_A_RX_DN	RX- of SATA Channel A	SATA

SATA_A_RX_DP	RX+ of SATA Channel A	SATA
SATA_A_TX_DN	TX- of SATA Channel A	SATA
SATA_A_TX_DP	TX+ of SATA Channel A	SATA
SATA_B_RX_DN	RX- of SATA Channel B	SATA
SATA_B_RX_DP	RX+ of SATA Channel B	SATA
SATA_B_TX_DN	TX- of SATA Channel B	SATA
SATA_B_TX_DP	TX+ of SATA Channel B	SATA
SATA_C_RX_DN	RX- of SATA Channel C	SATA
SATA_C_RX_DP	RX+ of SATA Channel C	SATA
SATA_C_TX_DN	TX- of SATA Channel C	SATA
SATA_C_TX_DP	TX+ of SATA Channel C	SATA
SATA_D_RX_DN	RX- of SATA Channel D	SATA
SATA_D_RX_DP	RX+ of SATA Channel D	SATA
SATA_D_TX_DN	TX- of SATA Channel D	SATA
SATA_D_TX_DP	TX+ of SATA Channel D	SATA
SerDes_A_RX_DN	Rx- of SerDes Channel A	SERDES
SerDes_A_RX_DP	Rx+ of SerDes Channel A	SERDES
SerDes_A_TX_DN	Tx- of SerDes Channel A	SERDES
SerDes_A_TX_DP	Tx+ of SerDes Channel A	SERDES
SerDes_B_RX_DN	Rx- of SerDes Channel B	SERDES
SerDes_B_RX_DP	Rx+ of SerDes Channel B	SERDES
SerDes_B_TX_DN	Tx- of SerDes Channel B	SERDES
SerDes_B_TX_DP	Tx+ of SerDes Channel B	SERDES
SerDes_C_RX_DN	Rx- of SerDes Channel A	SERDES
SerDes_C_RX_DP	Rx+ of SerDes Channel A	SERDES
SerDes_C_TX_DN	Tx- of SerDes Channel A	SERDES
SerDes_C_TX_DP	Tx+ of SerDes Channel A	SERDES
SerDes_D_RX_DN	Rx- of SerDes Channel B	SERDES
SerDes_D_RX_DP	Rx+ of SerDes Channel B	SERDES
SerDes_D_TX_DN	Tx- of SerDes Channel B	SERDES
SerDes_D_TX_DP	Tx+ of SerDes Channel B	SERDES
SLOT_ID_0	uModule ID Address 0	Slot ID
SLOT_ID_1	uModule ID Address 1	Slot ID
SLOT_ID_2	uModule ID Address 2	Slot ID
SLOT_ID_3	uModule ID Address 3	Slot ID
SLOT_ID_4	uModule ID Address 4	Slot ID
SLOT_ID_5	uModule ID Address 5	Slot ID
SMBus_CLK	Local SMBus Serial Clock	I2C Management
SMBus_DAT	Local SMBus Serial Data	I2C Management
USB_A_DN	USB Port A Data+	USB
USB_A_DP	USB Port A Data-	USB
USB_A_OC#	USB Port A Over Current	USB
USB_B_DN	USB Port B Data+	USB
USB_B_DP	USB Port B Data-	USB
USB_B_OC#	USB Port B Over Current	USB

3 Top Access µModule

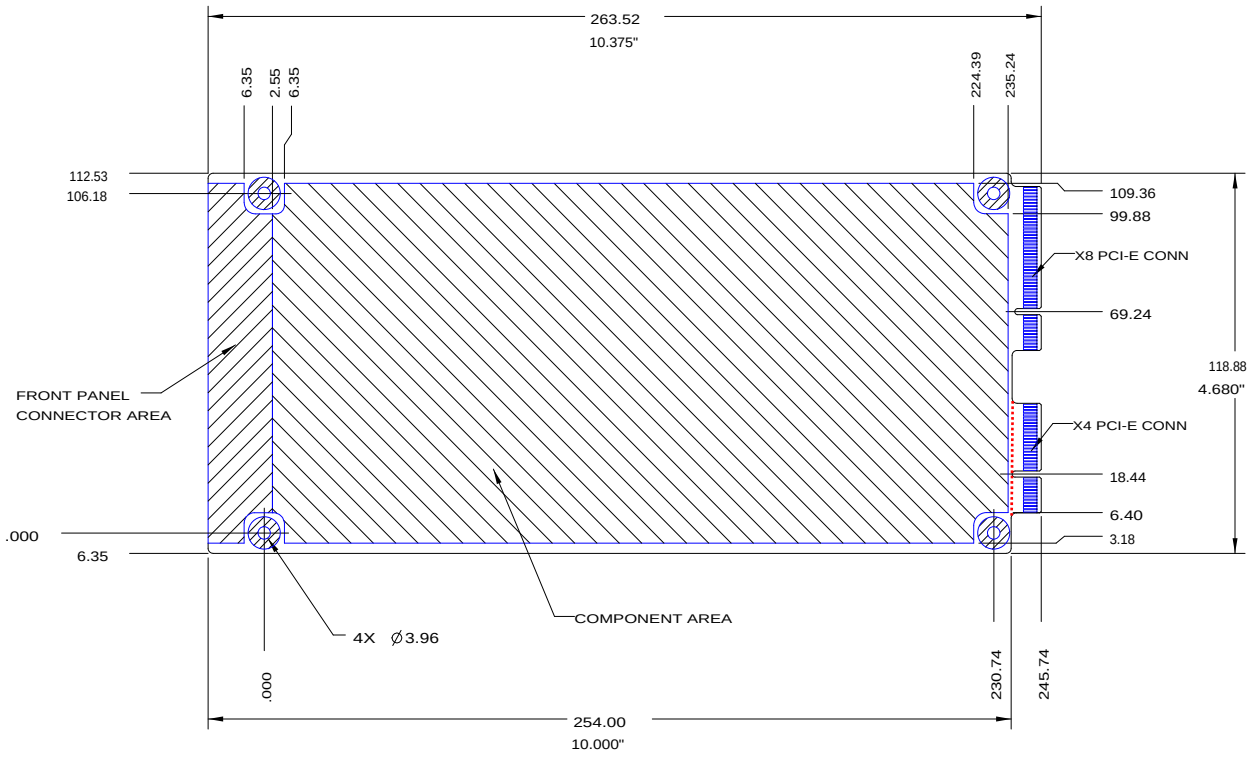
NOTICE: Redefinition of the Top Access µModule specification is in progress based on input from SSI contributors. Please contact the SSI Chairman for more details on the status of this specification.

4 Front Access µModule

4.1 Board Outline and Keepouts

In order to facilitate plugging of one or several µModule servers in the front of a chassis, the following form factor is specified. A face plate, insertion / extraction lever, and limited I/O would typically be present on the front panel (left side on the drawing below). The Front Access µModule PBA dimension **shall be** 4.680 inches x 10.375 inches, as shown in Figure 4-1. Figure 4-2 represents a physical view of a typical µModule PBA.

Figure 4-1: Front Access µModule PBA Dimensions



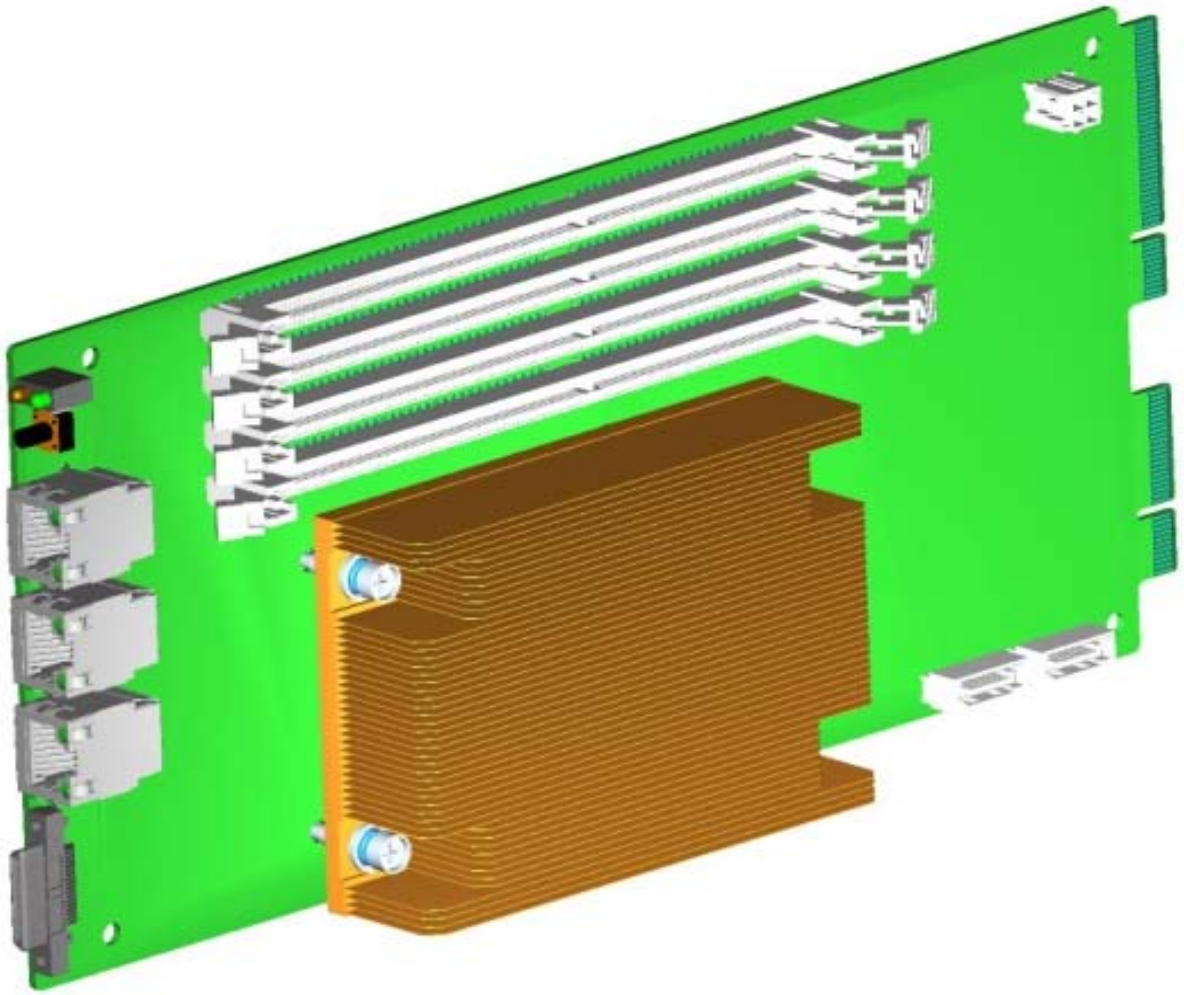
PRIMARY SIDE

Note: Dimensions in mm unless stated otherwise.

Note: The extended connector (x4 PCI-E) may be omitted. In this case the card edge aligns with the edge at the lower right corner (dotted line).

Note: The location of mounting holes is recommended.

Figure 4-2: Isometric View of Single-Node Front Access µModule (multi-node not shown).



4.1.1 PBA Thickness

The µModule PBA thickness is specified at 0.062" [1.57mm] ± 0.005". [0.13mm].

4.1.2 Primary Side Component Height

The *primary* side of the µModule contains the processor and memory. The maximum component height is dependent on the system design and the desired module to module pitch within the system.

For designs using standard DIMMs (1U enabled components), the recommended maximum component height is 1.378" [35.00mm]

For designs using Very Low Profile (VLP) DIMMs, the recommended maximum component height is 0.897" [22.78mm].

For designs using horizontal SO-DIMMs, the recommended maximum component height is 0.362" [9.20mm].

4.1.3 Secondary Side Component Height

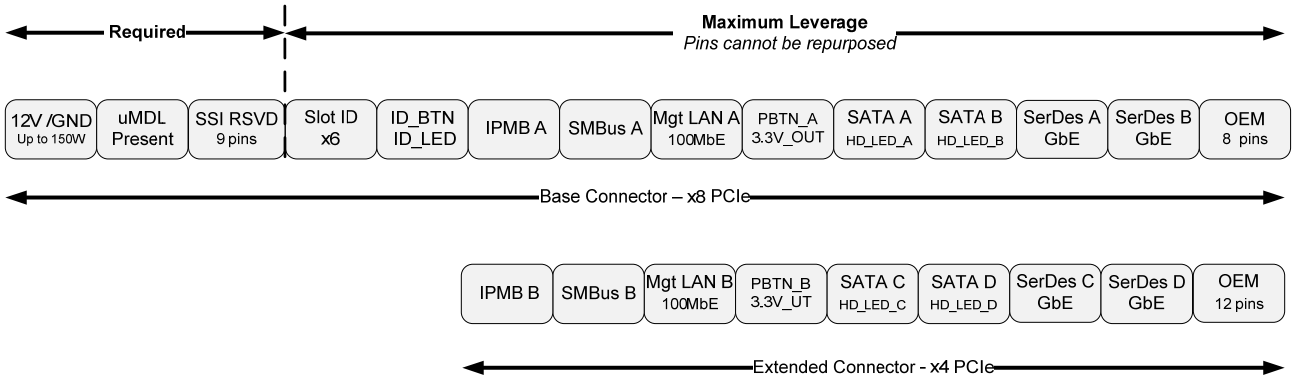
The *secondary* side of the µModule PBA is the side opposite the processor and memory. The **maximum** component height **shall** not exceed 0.125" [3.18mm].

4.2 Front Access µModule Connector Specification

4.2.1 Connector Overview

Figure 4-3 below provides a logical overview of the front access µModule connector.

Figure 4-3: Front Access µModule Connector Diagram



The front access µModule uses an edge finger connector derived from the PCI Express Specifications. Two physical PCIe connectors may be used; a base (x8) connector and an extended (x4) connector.

The "Base" connector **shall** be present for all µModules and has the same mechanical definition as the 98 pin x8 PCIe connector defined the PCIe specifications.

Within the Base section the following functions are required to be implemented as specific:

- 12V Power delivery supporting 150 W.
- Module Present pins
- Reserved (RSVD) pins for future specification use

The remaining functions are optional for any given implementation however it is recommended that all be implemented for maximum design leverage. Only pins designated OEM/Future use may be repurposed for other functions.

- Slot IDs to uniquely identify each µModule in a system
- Two I2C busses (IPMB and SMBus). See section 2.3.8 for a description of how these busses can be used.
- 2x SATA ports to access external storage
- 2x SERDES links which can be routed to internal network switches or PHY interfaces
- 1x dedicated Mngt LAN
- 7 pins for OEM specific functions and functions to be defined in a future revision.

The "Extended" connector (x4) **may** be present and provides for additional I/O and control needed in certain applications.

- 2x SATA ports to access additional storage
- 2x SERDES links for additional network ports
- Another set of I2C and Mngt LAN signals to support a second BMC on the module.

4.2.2 Connector Pinout

Table 4-1 shows the Base connector pinout, and Table 4-2 shows the Extended connector pinout

Note: Green color indicates ground connection and purple indicates 12V power connection. Blue pins are reserved, and light blue pins are reserved for OEM/Future use.

Table 4-1: Front Access Base Connector Pinout

Signal	Pin		Signal
PRSNT1#	B49	A49	OEM/Future Use
SLOT_ID_0	B48	A48	SLOT_ID_4
SLOT_ID_1	B47	A47	SLOT_ID_5
SLOT_ID_2	B46	A46	GND
SLOT_ID_3	B45	A45	SerDes_A_RX_DP
GND	B44	A44	SerDes_A_RX_DN
SerDes_A_TX_DP	B43	A43	GND
SerDes_A_TX_DN	B42	A42	GND
GND	B41	A41	SerDes_B_RX_DP
GND	B40	A40	SerDes_B_RX_DN
SerDes_B_TX_DP	B39	A39	GND
SerDes_B_TX_DN	B38	A38	ID_BTN#
GND	B37	A37	PWRBTN_A#
OEM/Future Use	B36	A36	ID_LED#
SMBus_A_CLK	B35	A35	OEM/Future Use
SMBus_A_DAT	B34	A34	OEM/Future Use
GND	B33	A33	IPMB_A_CLK
MNGT_A_TX_DP	B32	A32	IPMB_A_DATA
MNGT_A_TX_DN	B31	A31	GND
GND	B30	A30	MNGT_A_RX_DP
OEM/Future Use	B29	A29	MNGT_A_RX_DN
HDD_B_LED#	B28	A28	GND
HDD_A_LED#	B27	A27	OEM/Future Use
RSVD	B26	A26	OEM/Future Use
RSVD	B25	A25	OEM/Future Use
RSVD	B24	A24	RSVD
RSVD	B23	A23	RSVD
GND	B22	A22	3.3V_OUT_A
SATA_A_TX_DP	B21	A21	RSVD
SATA_A_TX_DN	B20	A20	GND
GND	B19	A19	SATA_A_RX_DP
GND	B18	A18	SATA_A_RX_DN
SATA_B_TX_DP	B17	A17	GND
SATA_B_TX_DN	B16	A16	GND
GND	B15	A15	SATA_B_RX_DP
RSVD	B14	A14	SATA_B_RX_DN
RSVD	B13	A13	GND
12V	B12	A12	PRSNT0#

KEY	KEY		KEY
12V	B11	A11	GND
12V	B10	A10	GND
12V	B9	A9	GND
12V	B8	A8	GND
12V	B6	A7	GND
12V	B6	A6	GND
12V	B5	A5	GND
12V	B4	A4	GND
12V	B3	A3	GND
12V	B2	A2	GND
12V	B1	A1	GND

Table 4-2 Front Access Extended Connector Pinout

Signal	Pin		Signal
PWRBTN_B#	B32	A32	OEM/Future Use
3.3V_OUT_B	B31	A31	GND
GND	B30	A30	SerDes_C_RX_DP
GND	B29	A29	SerDes_C_RX_DN
SerDes_C_TX_DP	B28	A28	GND
SerDes_C_TX_DN	B27	A27	GND
GND	B26	A26	SerDes_D_RX_DP
GND	B25	A25	SerDes_D_RX_DN
SerDes_D_TX_DP	B24	A24	GND
SerDes_D_TX_DN	B23	A23	GND
GND	B22	A22	MNGT_B_RX_DP
GND	B21	A21	MNGT_B_RX_DN
MNGT_B_TX_DP	B20	A20	GND
MNGT_B_TX_DN	B19	A19	IPMB_B_CLK
GND	B18	A18	IPMB_B_DATA
SMBus_B_CLK	B17	A17	OEM/Future Use
SMBus_B_DAT	B16	A16	OEM/Future Use
OEM/Future Use	B15	A15	OEM/Future Use
OEM/Future Use	B14	A14	OEM/Future Use
OEM/Future Use	B13	A13	OEM/Future Use
OEM/Future Use	B12	A12	OEM/Future Use
KEY	KEY		KEY
OEM/Future Use	B11	A11	HDD_D_LED#
GND	B10	A10	HDD_C_LED#

SATA_C_TX_DP	B9	A9	GND
SATA_C_TX_DN	B8	A8	GND
GND	B7	A7	SATA_C_RX_DP
GND	B6	A6	SATA_C_RX_DN
SATA_D_TX_DP	B5	A5	GND
SATA_D_TX_DN	B4	A4	GND
GND	B3	A3	SATA_D_RX_DP
GND	B2	A2	SATA_D_RX_DN
OEM/Future Use	B1	A1	GND

4.3 Front Access µModule Power Requirements

The front access µModule supports a power envelope of 150W. All power to the module is provided through the 12V pins. The Module **shall** draw a maximum of 12.5A from the 12V rail.

There is a 3.3V_OUT pin that a module may support. It shall provide 1A.

4.4 Connector Mechanical Specification

The front access µModule edge connectors are modeled after the PCI Express connector specified in *PCI Express® Card ElectroMechanical Specification Revision 2.0.* The 98 edge fingers in the µModule base connector are specified the same as the x8 I/O Card in section 5.2 (Connector Interface Definitions) of that document.

The 64 edge fingers in the µModule extended connector are specified the same as the x4 I/O Card in section 5.2 (Connector Interface Definitions) of that document.

The gold edge finger contacts **shall** conform to the same specifications as the PCI Express specification. Two pins on the µModule's base connector are shortened contacts to provide last mate / first break functionality:

- PRSNT0# (pin A12)
- PRSNT1# (pin B49)

These two contacts **shall** conform to the same specification as pin A1 of the PCI Express specification.

4.4.1 Connector Receptacles

The front access µModule typically plugs into a vertical backplane or midplane. PCIe x8 and PCIe x4connectors are standard in the industry and are available from multiple suppliers.

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5 Product Regulations Compliance

The SSI Micro Module Server **shall** meet regulatory requirements as governed by specific country regulations.